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Triode Emulator

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ABSTRACT

The design for a low-noise amplifier is presented. The amplifier has a tube-like transfer characteristic and produces harmonic distortion components that are similar to triode preamplifier.

0 INTRODUCTION

The static transfer characteristics of the vacuum tube follow the three halves power law. This determines the distortion characteristics of tube amplifier. Modest amount of feedback does not allow one to achieve good linearity in many tube amplifiers. This is especially true when triode-based musical instrument preamplifiers without overall feedback are taken into consideration. Harmonic analysis for such amplifiers shows regularity in the production of each successive harmonic [1,2]. The second harmonic usually dominates, followed closely by the third. The higher harmonics rise with input level running parallel to the second and the third.

There is a close relation between tube amplifier distortion and musical tone coloration [1]. A spectrum of harmonics, generated by a tube amplifier before the clipping region gives a full-bodied quality of sound. The audible difference between tube and solid-state amplifiers when they are clipped will not be discussed in this paper. That difference is described in [3]. The tube 'sound' and tube amplifiers 'musicality' is the phenomenon that has a real existence [4]. In this paper consideration is given to a voltage amplifier employing a common source gain stage with local current feedback, and a highly linear current-to-voltage converter. It will be demonstrated that it is possible to construct an amplifier with a tube-like transfer characteristic.

1 TUBE DISTORTION

The following equation for the vacuum triode plate current can be found in textbooks:

$$I_p = k(V_p + \mu V_g)^{3/2} \qquad (1)$$

where

I_p - is plate voltage,

V_g - is negative grid voltage,

μ - is amplification factor and

k - is dependent on tube geometry.

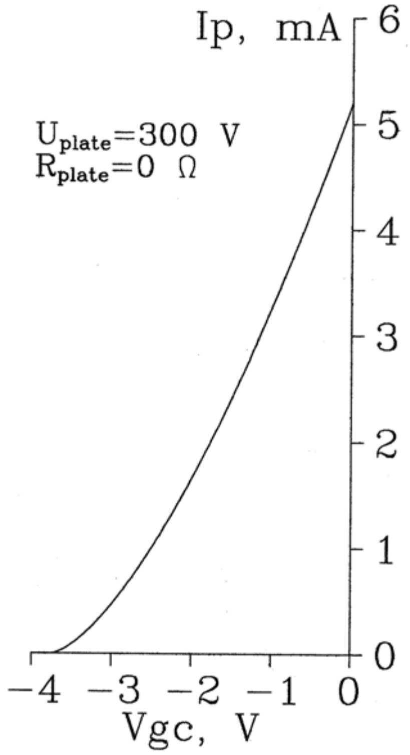

Fig.1. Typical vacuum triode transfer characteristic.

The typical transfer characteristic is presented in Fig.l. When $V_g = -V_p / \mu$ the plate current I_p becomes equal to zero and the tube cuts off. If a triode stage with a resistive load is taken into account then $V_p = E_p - I_p R_p$. Combining this with Eq.1 one can get a system of nonlinear equations for feedback stage [5]. With high plate load resistance the internal feedback [5] will be effective and will linearize ideal three halves law.

It is instructive to plot individual distortion curves for triode plate current in the assumption of ideal power law dependence (Eq.l). The input level is normalized on the maximum input grid AC voltage when plate current reaches zero. The working point is chosen exactly in the center of the input working range. The range is bounded by $V_g = -V_p / \mu$, below which the tube cuts-off and 0. At positive input voltages the grid current starts to flow. The analysis (Fig.2) shows the regularity in the production of each successive harmonic in plate current. It is very similar to the measured data [2] for the triode single stage design without feedback. The calculated data were obtained with V_p =300V, μ =80, $k = 1\,\mu A / V^{3/2}$, DC grid voltage is equal to -1.875 V. These values are typical for low power triodes.

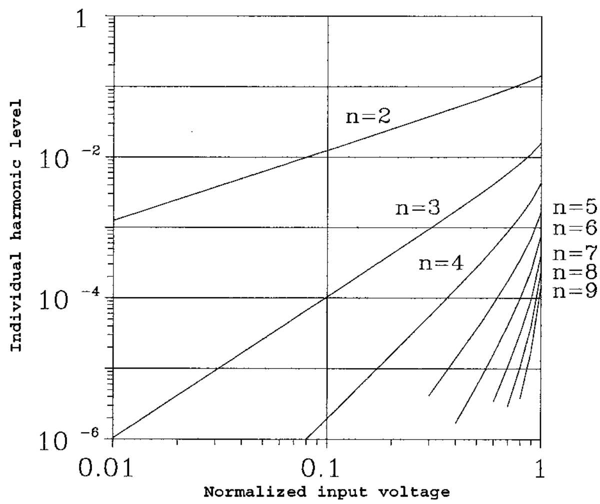

Fig.2. Calculated distortion products for vacuum triode plate current, assuming an ideal three-halves power law transfer characteristic.

2 FET DISTORTION

A field-effect transistor (FET) follows the parabo1ic relationship, as illustrated in Fig.3 (curve 1)

$$I_d = I_{dss} (V_{gs} / V_{(p)gs} - 1)^2 \qquad (2)$$

where

I_d - is drain current,

V_{gs} - is gate to source voltage,

$V_{(p)gs}$ - is pinch-off voltage and

I_{dss} - is drain current with gate and source tied together.

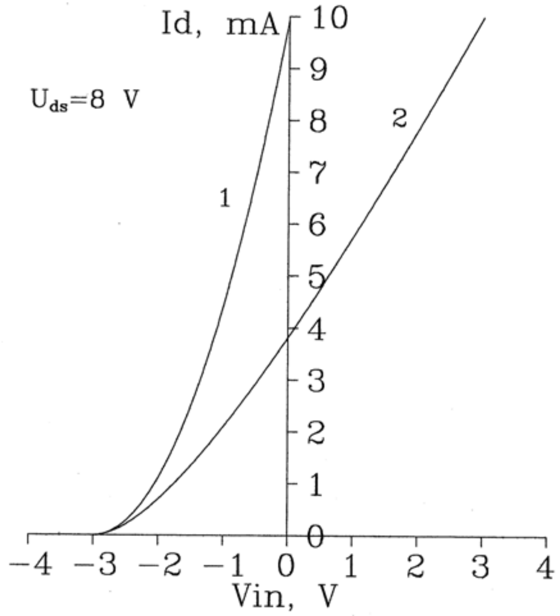

Fig.3. Transfer characteristics of a JFET. (1) - nearly ideal parabolic relationship without source resistor. (2) with local current feedback. Value of the source resistor is equal to $0.83 V_{(p)gs} / I_{dss} = 250\Omega$.

By applying negative feedback to a single FET stage, it is possible to linearize the transfer characteristic. With an increase in loop gain the resultant transfer function becomes more linear.

If a moderate amount of feedback is applied, a certain part of the FET stage transfer function will follow the three-halves power law. This is the intermediate case between ideal parabola and perfect straight line. For the FET stage with source resistor R_s one can write

$$I_d = I_{dss}(V_{gs}/V_{(p)gs} - 1)^2 \quad (3)$$

$$V_{in} = I_d R_s + V_{gs} \quad (4)$$

The drain-source voltage is assumed rather high to ensure FET to operate in the saturation region. Resolving the system (3,4) one can get:

$$V_{gs}^2 \frac{I_{dss} R_s}{V_{(p)gs}^2} + V_{gs}\left(1 - \frac{2 I_{dss} R_s}{V_{(p)gs}}\right) + \left(I_{dss} R_s - V_{in}\right) = 0 \quad (5)$$

denoting $1 - \frac{V_{(p)ss}}{2 I_{dss} R_s} = \chi$ for the simplicity

$$V_{gs} = \frac{-\chi + \sqrt{\chi^2 - 4\frac{I_{dss} R_s}{V_{(p)gs}^2}\left(I_{dss} R_s - V_{in}\right)}}{\frac{I_{dss} R_s}{V_{(p)gs}^2}} \quad (6)$$

$$I_d = \frac{V_{in} - V_{gs}}{R_s} = $$

$$= \frac{V_{in}}{R_s} + \frac{\chi - \sqrt{\chi^2 - 4\frac{I_{dss} R_s}{V_{(p)gs}^2}\left(I_{dss} R_s - V_{in}\right)}}{\frac{I_{dss} R_s^2}{V_{(p)gs}^2}} \quad (7)$$

It seems informative to plot the normalized drain current versus normalized input voltage for different values of R_s. The resulting set of curves is shown in Fig.4.

Horizontal scale is the normalized input voltage $\frac{V_{in} - V_{(p)gs}}{I_{dss} R_s - V_{(p)gs}}$:

$\frac{V_{in} - V_{(p)gs}}{I_{dss} R_s - V_{(p)gs}} = 0$, when $V_{in} = V_{(p)gs}$ and

$\frac{V_{in} - V_{(p)gs}}{I_{dss} R_s - V_{(p)gs}} = 1$, when $V_{gs} = 0$ ($V_{in} = I_{dss} R_s$).

Within this input rage the JFET gate is reverse biased. $\frac{V_{in} - V_{(p)gs}}{I_{dss} R_s - V_{(p)gs}} = \frac{1}{2}$ is a *dc* working point.

Vertical scale is the normalized drain current $\frac{I_d}{I_{dss}}$:

$\frac{I_d}{I_{dss}} = 0$, when $I_d = 0$ and $\frac{I_d}{I_{dss}} = 1$, when $I_d = I_{dss}$.

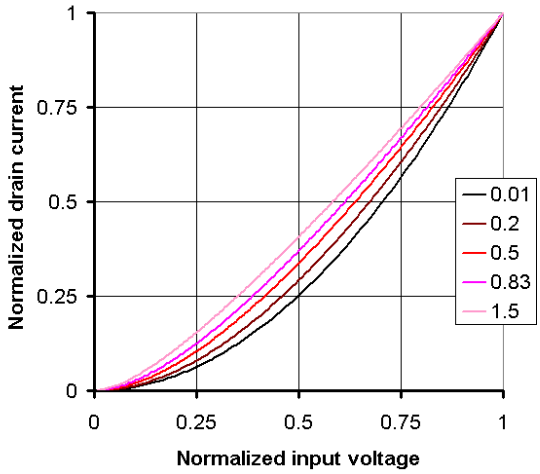

Fig.4. Normalized transfer characteristics of a JFET with source resistor, with $k = R_s \frac{I_{dss}}{V_{(p)gs}}$ as parameter.

Let us assume that for the small deviations the drain current deviation ΔI_d raised in the n power of input voltage deviation ΔV_{in}: $\Delta I_d = (\Delta V_{in})^n$. To obtain the required exponent value one can take the double logarithm of the normalized transfer characteristics (Fig.4) and then differentiate them. The result is shown in Fig.5

It is clear from Fig.5, that the transfer characteristic of JFET common source stage with a local feedback resistor R_s, connected between FET source and ground will be described by the three-halves power law in the vicinity of the *dc* working point when

$$R_s = 0.83 \frac{V_{(p)gs}}{I_{dss}} \quad (8)$$

If Eq.8 holds, then the *dc* gate voltage relative to ground is nearly zero and the input range of the FET stage is nearly symmetrical and bounded by $-V_{(p)gs}$ and $+V_{(p)gs}$ (Fig.3, curve 2).

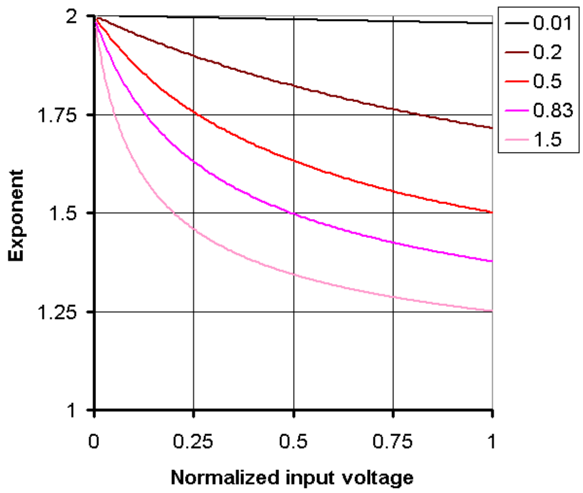

Fig.5. The exponent value n of the power dependence $\Delta I_d = (\Delta V_{in})^n$, with $k = R_s \frac{I_{dss}}{V_{(p)gs}}$ as parameter. The transfer characteristic corresponds most closely to three-halves (1.4 … 1.6) power law within one-third of the range of input signal when $R_s = 0.83 \frac{V_{(p)gs}}{I_{dss}}$.

Log-antilog techniques and analog multipliers are the alternative approaches to the construction of a gain stage with the tube-like transfer characteristic. Several circuits based on these principles have been built and tested. Poor noise performance and excessive level of high-order distortion products are their drawbacks.

3 CIRCUIT DESCRIPTIONS AND MEASURED PERFORMANCE

The complete circuit of the simulator is shown in Figs.8 and 9. The signal first passes through the input gain stage [6] and proceeds both to summing amplifier and FET common source stage. VR1 allows the gain to be adjusted to suit the level coming from the source before reaching the clipping point of the FET stage. The input stage gain can be varied with the LEVEL control from -8 dB to 28 dB.

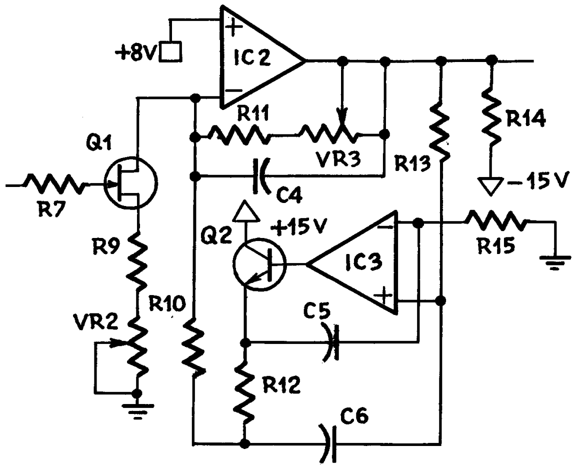

Fig.6. Common source FET stage loaded by I-V converter.

Operational amplifiers IC2 and IC3 form a highly linear current-to-voltage converter (Fig.6), which acts as a load to the FET stage and sets the gain. As the drain voltage of the FET is held at a constant level, the non1inearities associated with FET output network and gate-to-drain capacitance vanish. JFET has enough voltage across it to operate in the saturation region, while not that much to generate excessive noise due to reverse gate current. IC3 is used as a noninverting integrator in a servo feedback loop to ensure that the *dc* voltage at the output of the current-to-voltage converter remains close to the desired zero level. The IC3 stage works also as current source referring to the inverting input of IC2. The noise gain of IC2 in this case is equal to unity, as distinct from a previous circuit [7], where the noise contribution of IC2 was noticeable.

The output from the FET stage is mixed with a "dry" input signal in the output summing stage. The summing stage inputs come from highly correlated signal sources, it was designed with criterion that at the center of the EFFECT potentiometer (VR4) there would be no error in the sum of the source levels [8]. The output stage gain can be varied with the GAIN control from -32 dB to +8 dB. Special care was taken to minimize the residual distortion of operational amplifiers. Their output stages operate in class A due to resistor current sinks [9] (R8, R14, R21). The peak level detector (Fig.9) makes it possible to achieve maximum available rating from the FET stage and ensures that clipping is avoided.

The simulator can be inserted between a preamp1ifier and power amplifier or in the tape/effect send/return connection. The essentials are the LEVEL and the GAIN controls. At first the signal should be adjusted with the LEVEL potentiometer just before the LED begins to flash. After setting the output level with the GAIN control, the EFFECT control can be adjusted to add some amount of distortion to the original program material. In the end, the listener should judge the measure of sound coloration.

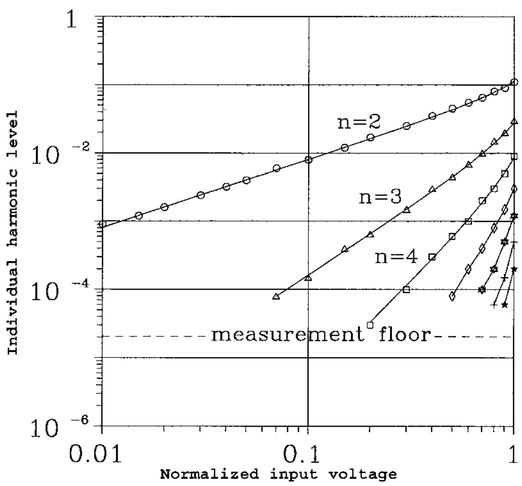

Fig.7. Measured results for Fig.6 circuit.

Several circuits were made in the form of tube simulator (Figs.8,9), active front-end electronics (Fig.6) [6] for various pick-ups (lead, bass guitar, etc) and microphone amplifiers (by addition the input transformer to Fig.6 circuit). Fig.7 displays the measured amplitude levels of the individual harmonics normalized to the fundamental for various input levels for the circuit shown in Fig.6. The FET parameters are $V_{(p)gs}$ = -3V, I_{dss} = 10mA, fundamental frequency 1 kHz. Notice that each harmonic dominates the next one with a higher number and each harmonic is reproduced with a regular rate of decrease. This effectively matches the estimated (Fig.2) and measured [1,2] data for vacuum triode stages.

Subjective testing has confirmed the psychoacoustic effect is "tubelike". The reproduction of the sound of acoustic guitars and violins has an impressive reality. One of a musicians reported that there is certain quality a tube amplifier must have and this design has not. It is the tubes. The reviewer could not peer inside the ventilation windows in the case and watch the tubes glow.

4 CONCLUSION

The design of a low-noise tube simulator is presented. An advantage of the region of the transfer function of the FET stage with local current feedback, which is closest to the three-halves power law, is taken. The design exhibits the tube-like transfer characteristics and the weighting of harmonics that are similar to those estimated and measured for triode type amplifiers. The circuit seems to be suitable for such application in the audio world as instrument/microphone amplifiers and special effect processors like aural stimulators.

5 ACKNOWLEDGEMENT

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APPENDIX

Table 1 - Parts list

Resistors

R1	56 kOhm
R2, R7, R16, R17, R18, R19, R23, R24, R25	10 kOhm
R3, R8, R14, R21	2.2 kOhm
R4	820 Ohm
R5, R6, R12	100 kOhm
R9	180 Ohm
R10	100 Ohm
R11, R22	390 Ohm
R13, R15, R27	1.6 Mohm
R20	4.7 kOhm
R26	1.6 kOhm

All resistors 1/4 W 5%.

Capacitors

C1, C7	10 uF, 50 V, nonpolar electrolytic
C2	100 uF, 25 V, electrolytic
C3	20 pF, 10%, ceramic
C4	560 pF, 10%, ceramic
C5, C6, C9	0.68 uF, 10%, 63 V, polyester
C8	5.1 pF, 10%, ceramic

Diodes

Dl, D2, D3, D4	1N914
Z1	Zener 8 V
Z2	Zener 4.7 V

Transistors

Q1	2N4416, 2N5270, 2N5459 or any small signal low-noise JFET
Q2	BC182 or any small-signal, low noise, n-p-n BJT

Integrated Circuits

IC1,IC2, IC3,IC4	LF351A (TL071C)
IC5	LM311
IC6	4069 hex CMOS invertor

Miscellaneous

VR1	47 kOhm, dual linear pot
VR2	470 Ohm, multiturn trimpot
VR3	2 kOhm, multiturn trimpot
VR4	1 kOhm dual linear pot
VR5	470 kO dual linear pot
VR6, VR7	10 kOhm, multiturn trimpot

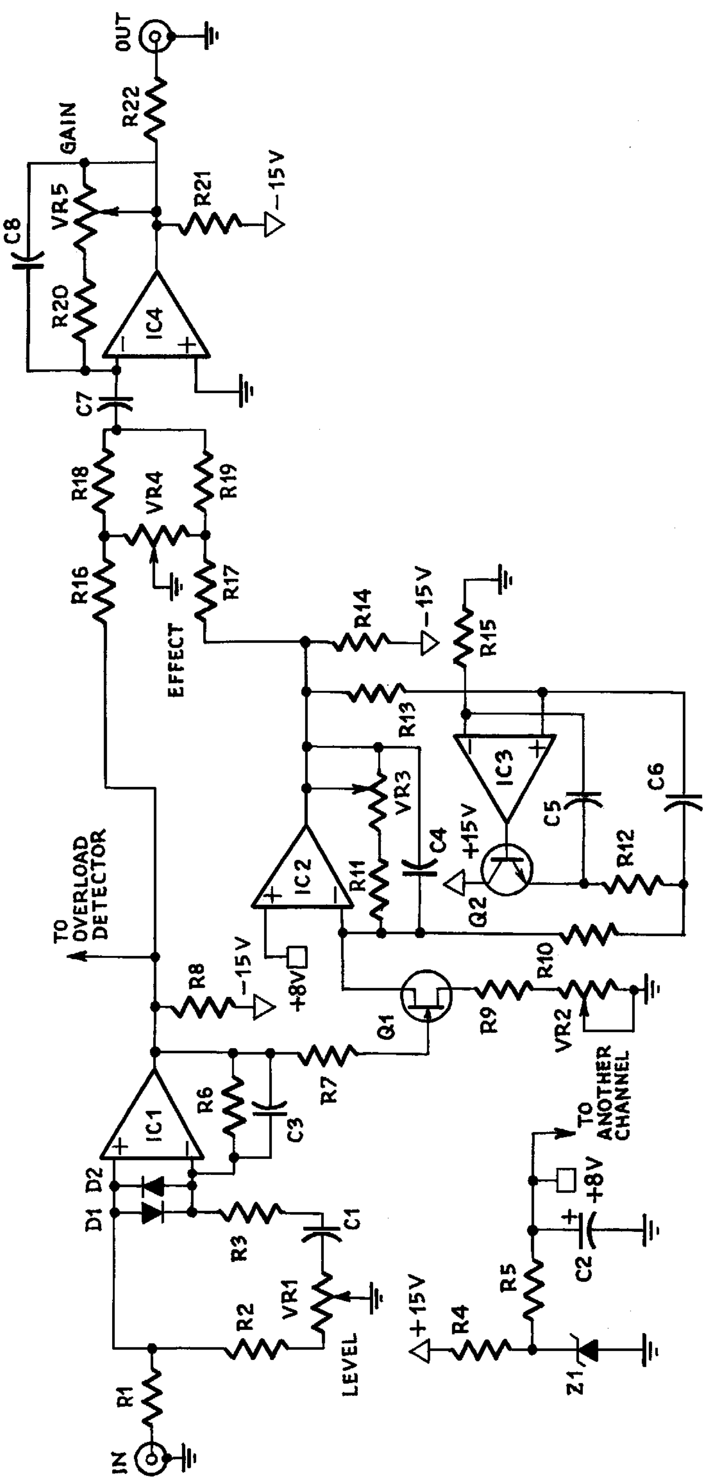

Fig.8. Triode simulator.

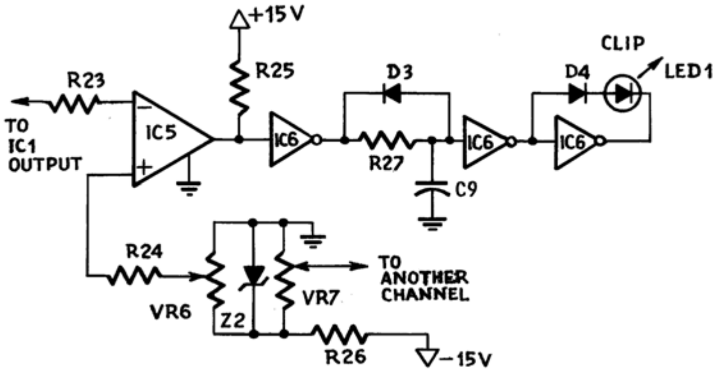

Fig.9. Overload detector.

Adjustment procedure

For the given FET two quantities should be measured: $V_{(p)gs}$ - gate-source cut-off voltage and I_{dss} - drain current with source short-circuited to gate. Then by VR2 the sum of VR2 and R9 is adjusted to be equal $0.83\frac{V_{(p)gs}}{I_{dss}}$. VR3 allows achieving the overall unity gain in FET stage, and the negative voltage on the slider of VR6 (VR7) is set to be equal $V_{(p)gs}$ for the reliable peak overload detection.

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